IN THE CLAIMS:

Please cancel claims 1-20, amend claims 21 and 24-26 and add new claims 27-37 as follows. Please note that claims 22-23 remain unchanged, but are reproduced for the Examiner's convenience and reference.

21. (Amended) A method of fabricating an integrated circuit comprising[**the steps of**]:

depositing a field implant;

depositing a well implant; and

depositing an enhancement implant, wherein the **[steps of]** depositing a field implant, depositing a well implant, and depositing an enhancement implant are done using a single mask.

22. (Unchanged) The method of claim 21 wherein the well implant is an n-well implant.

23. (Unchanged) The method of claim 21 wherein the well implant is a p-well implant.

24. (Amended) The method of claim 21 further comprising**[the steps of]**:

forming a high voltage native transistor by blocking the well implant and the enhancement implant; and

offsetting the field implant from an active area of the native transistor, thereby obtaining high gated-diode junction breakdown characteristics.

25. (Amended) The method of claim 21, further comprising**[the step of]** implanting a pocket implant to improve a punch-through immunity.

26. (Amended) The method of claim 21 further comprising**[the step of]**:

depositing two pocket implants; and

merging the pocket implants together by lateral diffusion, whereby a channel doping profile from the pocket implant diffusion exhibits reverse-short-channel effect.

Please add the following new claims:

--27. (New) A method of fabricating a transistor in integrated circuit device comprising:

providing a semiconductor substrate;

forming a gate oxide on the semiconductor substrate;

forming a gate on the gate oxide;

implanting a first pocket implant into the semiconductor substrate from a first side of the gate;

implanting a second pocket implant into the semiconductor substrate from a second side of the gate; and

diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate.

28. (New) The method of claim 27 wherein the first pocket implant is in contact with the second pocket implant.

29. (New) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted at an angle.

30. (New) The method of claim 27 wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

31. (New) The method of claim 27 wherein the diffusing increases a reverse short channel effect of the transistor.

32. (New) The method of claim 27 further comprising implanting an enhancement implant in the semiconductor substrate.

33. (New) The method of claim 27 further comprising forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.